AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A memory device couplable to a plurality of accessing devices, the memory device comprising:

a memory comprising a plurality of banks;

a plurality of ports for accessing the plurality of banks of the memory, each port having a bit serial communications link for receiving from and transmitting to an accessing device where bits of each symbol are received and transmitted serially, each port using a plesiosynchronous technique without transmitting a clock signal to receive symbols and using in-band symbols to transmit data and out-of-band symbols to transmit control information; and

a switch for selectively routing symbols between the plurality of ports and the plurality of banks, wherein the bits of symbols are routed by the switch in parallel.

2. (Previously Presented) The memory device of claim 1 wherein each bit serial communications link is connected to an accessing device via a point-to-point connection.

3. (Previously Presented) The memory device of claim 1 wherein the plesiosynchronous technique oversamples data received via the bit serial communications link.

4. (Previously Presented) A memory device comprising:

a memory; and

a plurality of ports for accessing the memory of the memory device, each port having a serial communications link for receiving from and transmitting to an accessing device, each port using plesiosynchronous technique to receive symbols and using in-band symbols to transmit data and out-of-band symbols to transmit control information wherein each port includes a line driver with a fixed driver portion and a variable driver portion for DC-balancing.

5. (Previously Presented) The memory device of claim 1 wherein the plurality of banks can be simultaneously accessed by different ports.

6. (Previously Presented) The memory device of claim 1 wherein each bank includes multiple sections and wherein the multiple sections can be simultaneously accessed by different ports.

7. (Canceled)

8. (Previously Presented) The memory device of claim 6 wherein the multiple sections of the bank are configurable on a port-by-port basis.

9. (Original) The memory device of claim 8 wherein the configuration information indicates to enable certain sections of the bank.

10. (Original) The memory device of claim 1 wherein the ports are connected to the memory using time-division multiplexing.

11. (Previously Presented) The memory device of claim 1 wherein the switch is a crossbar switch.

12. (Original) The memory device of claim 1 wherein control information is transmitted as a primitive.

13. (Original) The memory device of claim 12 wherein a primitive includes two out-of-band symbols.

14. (Original) The memory device of claim 12 wherein control information includes a synchronization symbol.

15. (Original) The memory device of claim 1 wherein the plesiosynchronous technique includes inserting or removing symbols to compensate for variations between clock frequencies of the accessing device and the memory device.

16. (Original) The memory device of claim 1 wherein the ports share a single multiphase clock generator.

17. (Original) The memory device of claim 16 wherein the multiphase clock generator is a phase lock loop.

18. (Original) The memory device of claim 1 wherein an out-of-band symbol is a synchronization symbol that encodes a memory command.

19. (Previously Presented) A memory device comprising: a memory comprising a plurality of banks that reads and writes data; a multiphase clock generator that provides a multiphase clock signal; a plurality of ports for accessing the plurality of banks, each port for connecting to a bit serial communications link, where bits of each symbol are received and transmitted serially, and for receiving data and control information via the bit serial communications link using a plesiosynchronous technique without transmitting a clock signal, wherein each port uses the generated multiphase clock signal generated by the

multiphase clock generator; and a switch for selectively routing symbols between the plurality of ports and the plurality of banks, wherein the bits of symbols are routed by the switch in parallel.

20. (Original) The memory device of claim 19 wherein data is sent using in-band symbols and control information is sent via out-of-band symbols.

21. (Previously Presented) The memory device of claim 19 wherein each bit serial communications link is connected to an accessing device via a point-to-point connection.

22. (Previously Presented) The memory device of claim 19 wherein the plesiosynchronous technique oversamples data received via the bit serial communications link.

23. (Previously Presented) A memory device comprising: a memory that reads and writes data; a multiphase clock generator that provides a multiphase clock signal; and a plurality of ports, each port for connecting to a serial communications link and for receiving data and control information via the serial communications link using a plesiosynchronous technique, wherein each port uses the generated multiphase clock signal generated by the multiphase clock generator and wherein each port includes a line driver with a fixed driver portion and a variable driver portion for DC-balancing.

24. (Previously Presented) The memory device of claim 19 wherein the plurality of banks can be simultaneously accessed by different ports.

25. (Previously Presented) The memory device of claim 19 wherein each bank includes multiple sections and wherein multiple sections can be simultaneously accessed by different ports.

26. (Canceled)

27. (Currently Amended) The memory device of claim ~~26~~25 wherein the multiple sections are configurable on a port-by-port basis.

28. (Original) The memory device of claim 27 including the configuration information storage.

29. (Original) The memory device of claim 19 wherein the ports are connected to the memory using time-division multiplexing.

30. (Previously Presented) The memory device of claim 19 wherein the switch is a crossbar switch.

31. (Original) The memory device of claim 19 wherein control information is transmitted as a primitive.

32. (Original) The memory device of claim 31 wherein a primitive includes two out-of-band symbols.

33. (Original) The memory device of claim 31 wherein control information includes a synchronization symbol.

34. (Original) The memory device of claim 19 wherein the plesiosynchronous technique includes inserting or removing symbols to compensate for variations between clock frequencies of the accessing device and the memory device.

35. (Original) The memory device of claim 19 wherein the multiphase clock generator is a phase lock loop.

36. (Original) The memory device of claim 19 wherein a synchronization symbol encodes a memory command.

37. – 40. (Canceled)